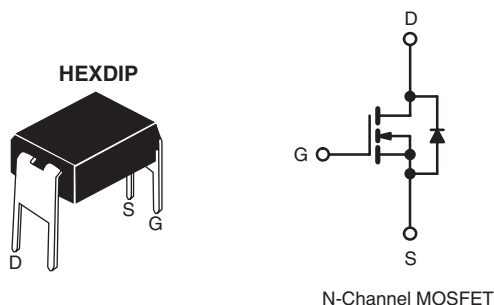


## Power MOSFET

### PRODUCT SUMMARY

|                           |                        |     |
|---------------------------|------------------------|-----|
| $V_{DS}$ (V)              | 200                    |     |
| $R_{DS(on)}$ ( $\Omega$ ) | $V_{GS} = 10\text{ V}$ | 1.5 |
| $Q_g$ (Max.) (nC)         | 8.2                    |     |
| $Q_{gs}$ (nC)             | 1.8                    |     |
| $Q_{gd}$ (nC)             | 4.5                    |     |
| Configuration             | Single                 |     |



### FEATURES

- Dynamic  $dV/dt$  Rating
- Repetitive Avalanche Rated
- For Automatic Insertion
- End Stackable
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Lead (Pb)-free Available



Available  
**RoHS\***  
COMPLIANT

### DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The 4 pin DIP package is a low cost machine-insertable case style which can be stacked in multiple combinations on standard 0.1" pin centers. The dual drain serves as a thermal link to the mounting surface for power dissipation levels up to 1 W.

### ORDERING INFORMATION

|                |                           |
|----------------|---------------------------|
| Package        | HEXDIP                    |
| Lead (Pb)-free | IRFD210PbF<br>SiHFD210-E3 |
| SnPb           | IRFD210<br>SiHFD210       |

### ABSOLUTE MAXIMUM RATINGS $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted

| PARAMETER                                        | SYMBOL                           | LIMIT                             | UNIT                |
|--------------------------------------------------|----------------------------------|-----------------------------------|---------------------|
| Drain-Source Voltage                             | $V_{DS}$                         | 200                               | V                   |
| Gate-Source Voltage                              | $V_{GS}$                         | $\pm 20$                          |                     |
| Continuous Drain Current                         | $V_{GS}$ at 10 V                 | $T_C = 25\text{ }^\circ\text{C}$  | A                   |
|                                                  |                                  | $T_C = 100\text{ }^\circ\text{C}$ |                     |
| Pulsed Drain Current <sup>a</sup>                | $I_{DM}$                         | 4.8                               |                     |
| Linear Derating Factor                           |                                  | 0.0083                            | W/ $^\circ\text{C}$ |
| Single Pulse Avalanche Energy <sup>b</sup>       | $E_{AS}$                         | 79                                | mJ                  |
| Repetitive Avalanche Current <sup>a</sup>        | $I_{AR}$                         | 0.60                              | A                   |
| Repetitive Avalanche Energy <sup>a</sup>         | $E_{AR}$                         | 0.10                              | mJ                  |
| Maximum Power Dissipation                        | $T_C = 25\text{ }^\circ\text{C}$ | $P_D$                             | W                   |
| Peak Diode Recovery $dV/dt$ <sup>c</sup>         | $dV/dt$                          | 5.0                               | V/ns                |
| Operating Junction and Storage Temperature Range | $T_J, T_{stg}$                   | - 55 to + 150                     | $^\circ\text{C}$    |
| Soldering Recommendations (Peak Temperature)     | for 10 s                         | 300 <sup>d</sup>                  |                     |

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 50\text{ V}$ , starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 82\text{ mH}$ ,  $R_G = 25\text{ }\Omega$ ,  $I_{AS} = 1.2\text{ A}$  (see fig. 12).
- $I_{SD} \leq 3.3\text{ A}$ ,  $dI/dt \leq 70\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150\text{ }^\circ\text{C}$ .
- 1.6 mm from case.

\* Pb containing terminations are not RoHS compliant, exemptions may apply

**THERMAL RESISTANCE RATINGS**

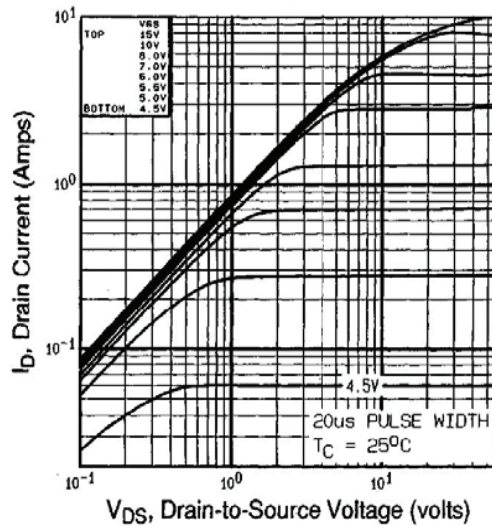
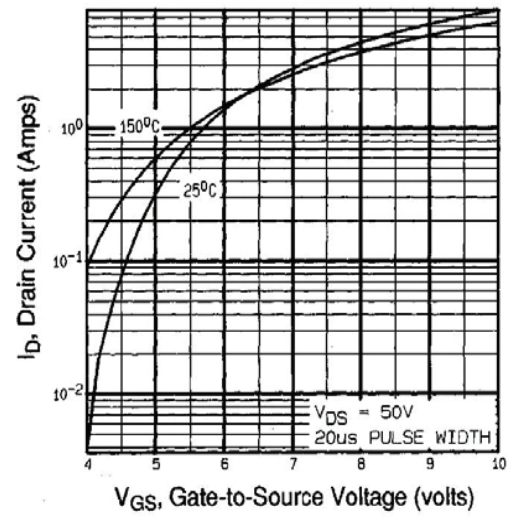
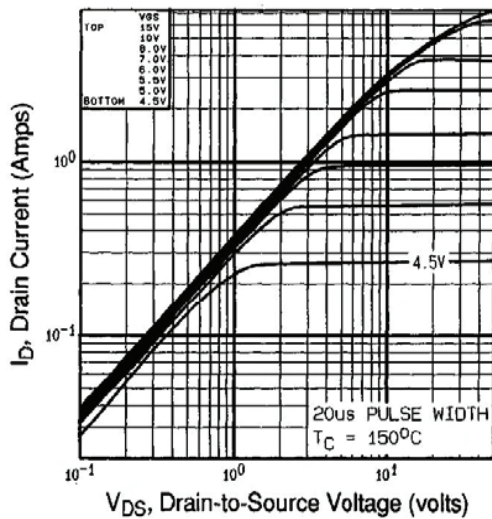
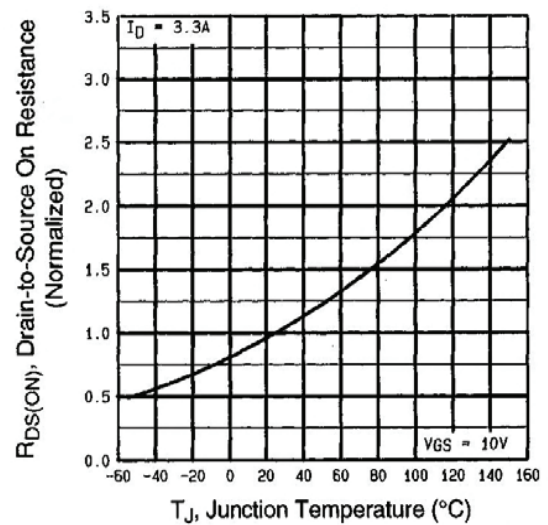
| PARAMETER                   | SYMBOL     | TYP. | MAX. | UNIT |
|-----------------------------|------------|------|------|------|
| Maximum Junction-to-Ambient | $R_{thJA}$ | -    | 120  | °C/W |

**SPECIFICATIONS**  $T_J = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted

| PARAMETER                                 | SYMBOL                           | TEST CONDITIONS                                                                                                           |                                                                                   | MIN. | TYP. | MAX.  | UNIT |
|-------------------------------------------|----------------------------------|---------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------|------|------|-------|------|
| Static                                    |                                  |                                                                                                                           |                                                                                   |      |      |       |      |
| Drain-Source Breakdown Voltage            | V <sub>DS</sub>                  | V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA                                                                            |                                                                                   | 200  | -    | -     | V    |
| V <sub>DS</sub> Temperature Coefficient   | ΔV <sub>DS</sub> /T <sub>J</sub> | Reference to 25 °C, I <sub>D</sub> = 1 mA                                                                                 |                                                                                   | -    | 0.30 | -     | V/°C |
| Gate-Source Threshold Voltage             | V <sub>GS(th)</sub>              | V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA                                                               |                                                                                   | 2.0  | -    | 4.0   | V    |
| Gate-Source Leakage                       | I <sub>GSS</sub>                 | V <sub>GS</sub> = ± 20 V                                                                                                  |                                                                                   | -    | -    | ± 100 | nA   |
| Zero Gate Voltage Drain Current           | I <sub>DSS</sub>                 | V <sub>DS</sub> = 200 V, V <sub>GS</sub> = 0 V                                                                            |                                                                                   | -    | -    | 25    | μA   |
|                                           |                                  | V <sub>DS</sub> = 160 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C                                                   |                                                                                   | -    | -    | 250   |      |
| Drain-Source On-State Resistance          | R <sub>DS(on)</sub>              | V <sub>GS</sub> = 10 V                                                                                                    | I <sub>D</sub> = 0.36 A <sup>b</sup>                                              | -    | -    | 1.5   | Ω    |
| Forward Transconductance                  | g <sub>fs</sub>                  | V <sub>DS</sub> = 50 V, I <sub>D</sub> = 0.36 A <sup>b</sup>                                                              |                                                                                   | 0.10 | -    | -     | S    |
| Dynamic                                   |                                  |                                                                                                                           |                                                                                   |      |      |       |      |
| Input Capacitance                         | C <sub>iss</sub>                 | V <sub>GS</sub> = 0 V<br>V <sub>DS</sub> = 25 V<br>f = 1.0 MHz, see fig. 5                                                |                                                                                   | -    | 140  | -     | pF   |
| Output Capacitance                        | C <sub>oss</sub>                 |                                                                                                                           |                                                                                   | -    | 53   | -     |      |
| Reverse Transfer Capacitance              | C <sub>rss</sub>                 |                                                                                                                           |                                                                                   | -    | 15   | -     |      |
| Total Gate Charge                         | Q <sub>g</sub>                   | V <sub>GS</sub> = 10 V                                                                                                    | I <sub>D</sub> = 3.3 A, V <sub>DS</sub> = 160 V<br>see fig. 6 and 13 <sup>b</sup> | -    | -    | 8.2   | nC   |
| Gate-Source Charge                        | Q <sub>gs</sub>                  |                                                                                                                           |                                                                                   | -    | -    | 1.8   |      |
| Gate-Drain Charge                         | Q <sub>gd</sub>                  |                                                                                                                           |                                                                                   | -    | -    | 4.5   |      |
| Turn-On Delay Time                        | t <sub>d(on)</sub>               | V <sub>DD</sub> = 100 V, I <sub>D</sub> = 3.3 A<br>R <sub>G</sub> = 24 Ω, R <sub>D</sub> = 30 Ω, see fig. 10 <sup>b</sup> |                                                                                   | -    | 8.2  | -     | ns   |
| Rise Time                                 | t <sub>r</sub>                   |                                                                                                                           |                                                                                   | -    | 17   | -     |      |
| Turn-Off Delay Time                       | t <sub>d(off)</sub>              |                                                                                                                           |                                                                                   | -    | 14   | -     |      |
| Fall Time                                 | t <sub>f</sub>                   |                                                                                                                           |                                                                                   | -    | 8.9  | -     |      |
| Internal Drain Inductance                 | L <sub>D</sub>                   | Between lead,<br>6 mm (0.25") from<br>package and center of<br>die contact                                                |                                                                                   | -    | 4.0  | -     | nH   |
| Internal Source Inductance                | L <sub>S</sub>                   |                                                                                                                           |                                                                                   | -    | 6.0  | -     |      |
| Drain-Source Body Diode Characteristics   |                                  |                                                                                                                           |                                                                                   |      |      |       |      |
| Continuous Source-Drain Diode Current     | I <sub>S</sub>                   | MOSFET symbol<br>showing the<br>integral reverse<br>p - n junction diode                                                  |                                                                                   | -    | -    | 0.60  | A    |
| Pulsed Diode Forward Current <sup>a</sup> | I <sub>SM</sub>                  |                                                                                                                           |                                                                                   | -    | -    | 4.8   |      |
| Body Diode Voltage                        | V <sub>SD</sub>                  | T <sub>J</sub> = 25 °C, I <sub>S</sub> = 0.60 A, V <sub>GS</sub> = 0 V <sup>b</sup>                                       |                                                                                   | -    | -    | 2.0   | V    |
| Body Diode Reverse Recovery Time          | t <sub>rr</sub>                  | T <sub>J</sub> = 25 °C, I <sub>F</sub> = 3.3 A, dI/dt = 100 A/μs <sup>b</sup>                                             |                                                                                   | -    | 150  | 310   | ns   |
| Body Diode Reverse Recovery Charge        | Q <sub>rr</sub>                  |                                                                                                                           |                                                                                   | -    | 0.60 | 1.4   | μC   |
| Forward Turn-On Time                      | t <sub>on</sub>                  | Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> and L <sub>D</sub> )                         |                                                                                   |      |      |       |      |

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)  
b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

**Fig. 1 - Typical Output Characteristics,  $T_C = 25^\circ\text{C}$** 

**Fig. 3 - Typical Transfer Characteristics**

**Fig. 2 - Typical Output Characteristics,  $T_C = 150^\circ\text{C}$** 

**Fig. 4 - Normalized On-Resistance vs. Temperature**

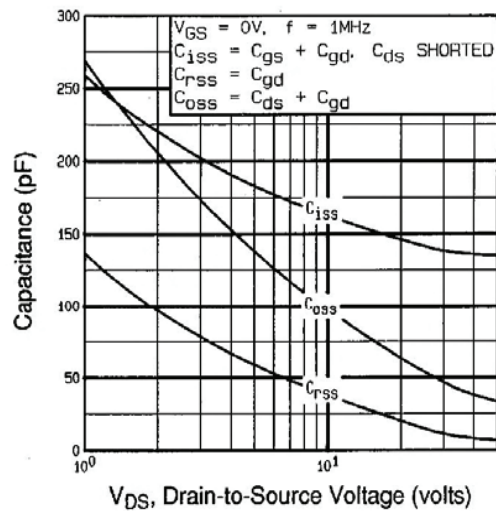


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

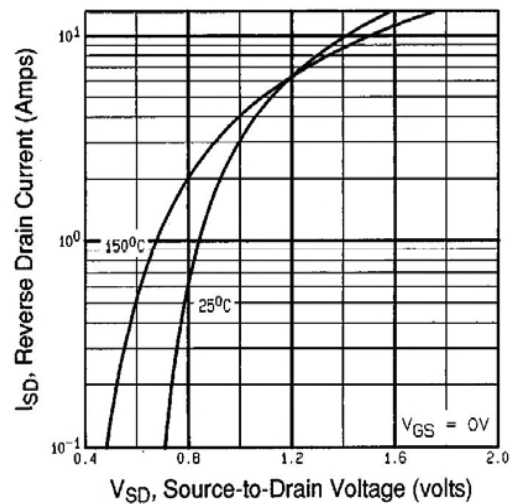


Fig. 7 - Typical Source-Drain Diode Forward Voltage

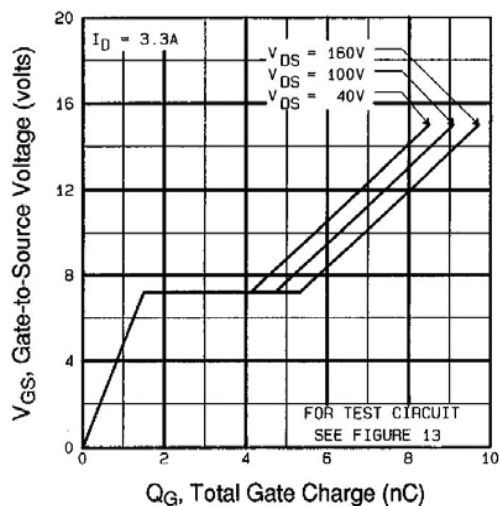


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

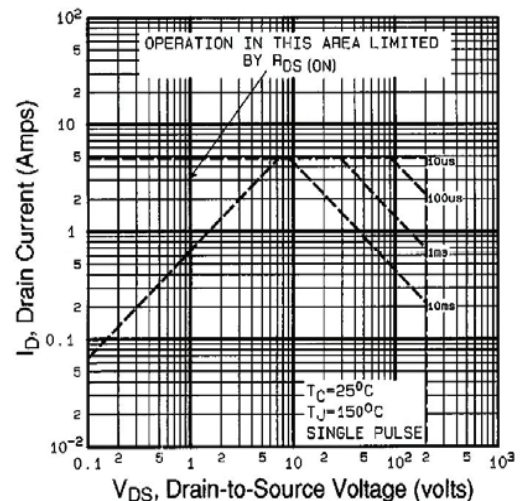


Fig. 8 - Maximum Safe Operating Area

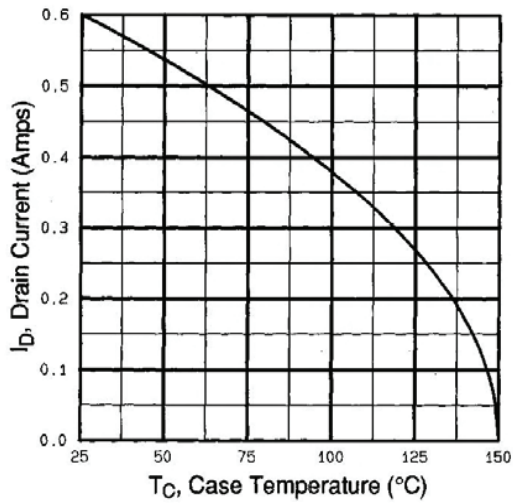


Fig. 9 - Maximum Drain Current vs. Case Temperature

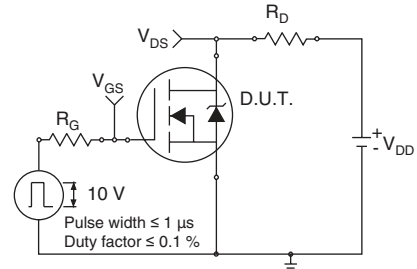


Fig. 10a - Switching Time Test Circuit

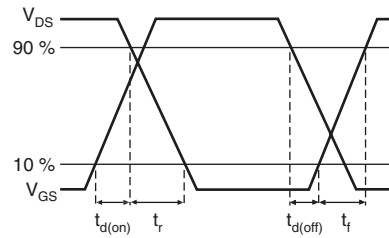


Fig. 10b - Switching Time Waveforms

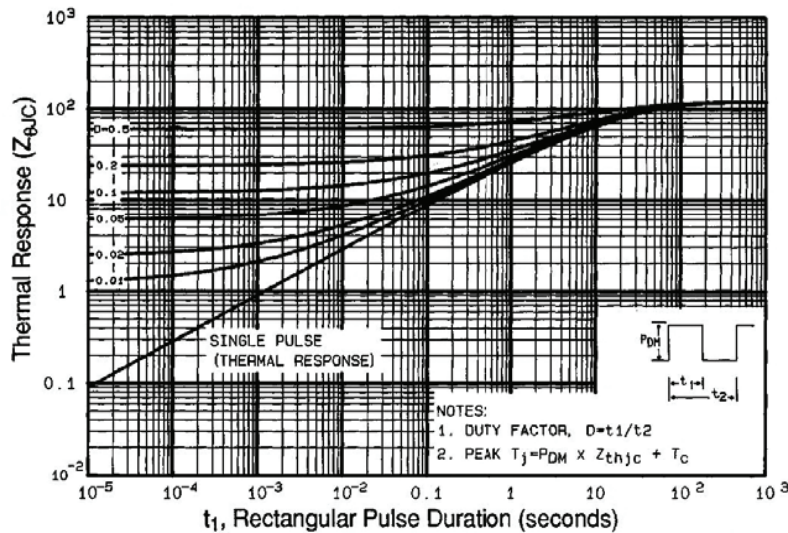


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

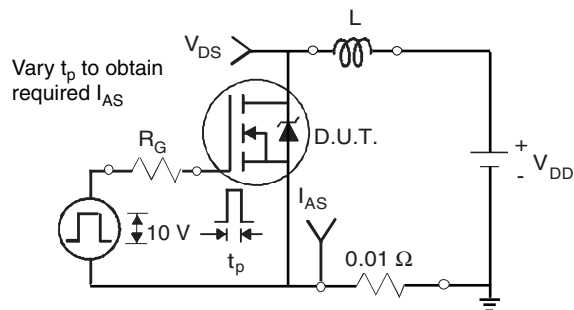


Fig. 12a - Unclamped Inductive Test Circuit

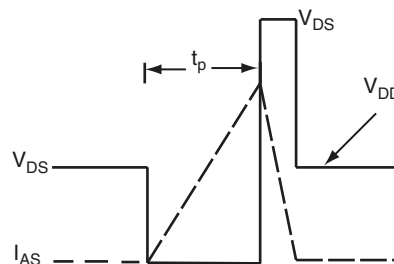


Fig. 12b - Unclamped Inductive Waveforms

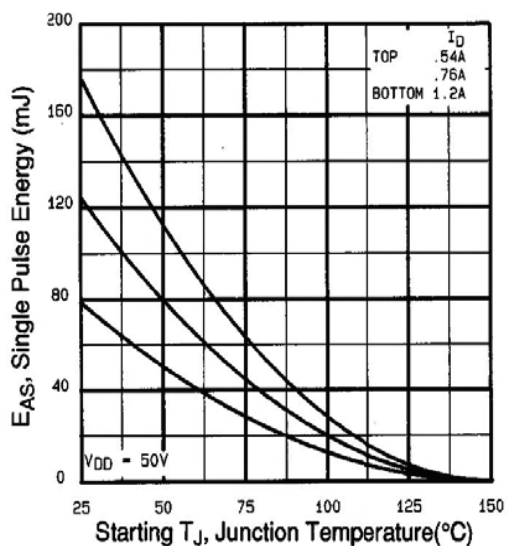


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

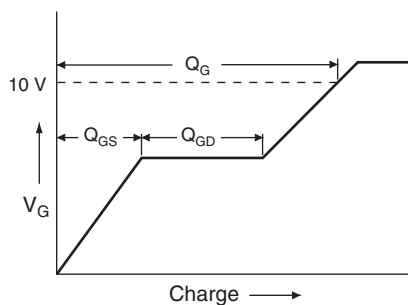


Fig. 13a - Basic Gate Charge Waveform

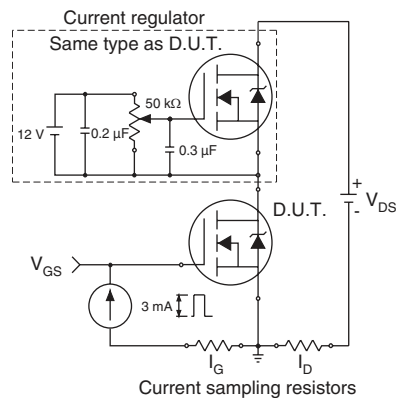
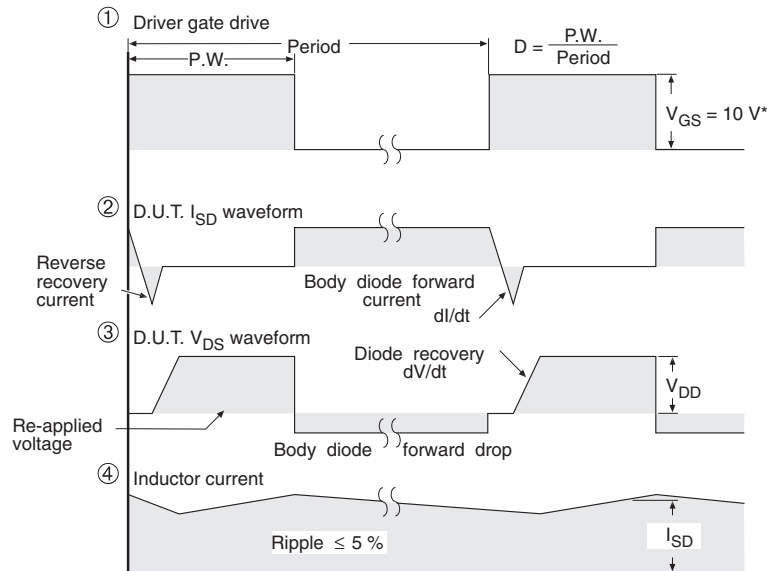
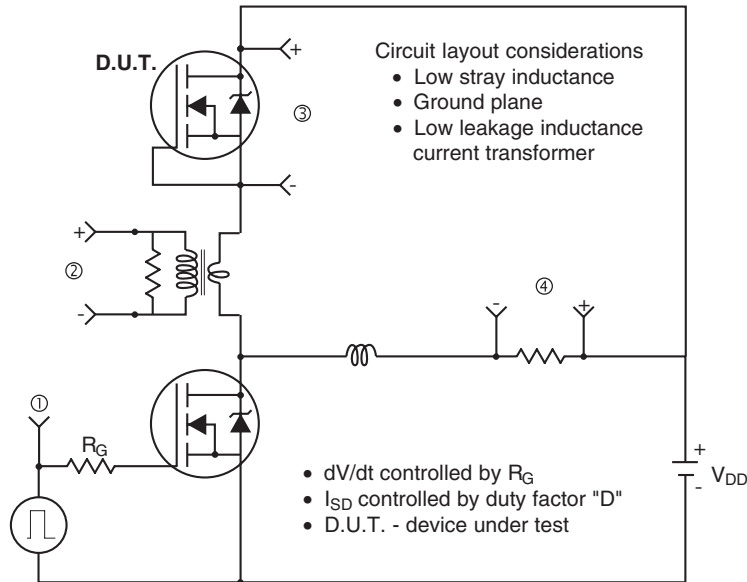


Fig. 13b - Gate Charge Test Circuit

## Peak Diode Recovery $dV/dt$ Test Circuit



\*  $V_{GS} = 5 V$  for logic level devices and  $3 V$  drive devices

**Fig. 14 - For N-Channel**

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